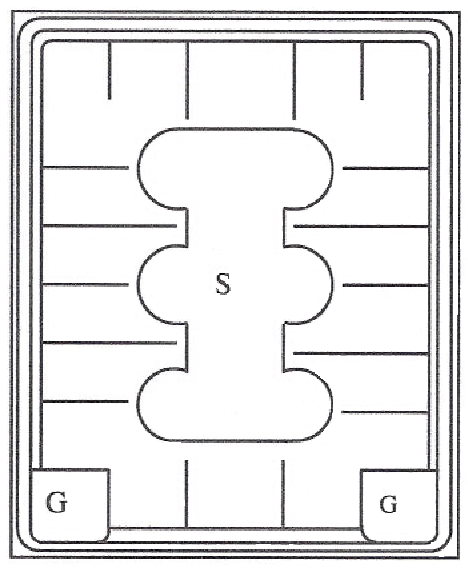
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.283”**



**.348”**

**Top Material: Al**

**Backside Material: TiNiAu**

**Bond Pad Size: G=43x43, S=197x126**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .283” X .348” DATE: 7/19/21**

**MFG: IXYS THICKNESS .012” P/N: IXTD11P50**

**DG 10.1.2**

#### Rev B, 7/19/02